

CLAIMS

We claim:

- 1 1. A method for facilitating high signal throughput of an improved CMOS image sensor
2 comprising a plurality of photo sensors configured in a two-dimensional array; said
3 method comprising:
4 generating column address signals and row address signals that address a subset of
5 said two-dimensional array according to a set of parameters; and
6 reading out charge signals from a set of the plurality of photo sensors in said
7 image sensor; said set of photo sensors addressed by said column address
8 signals and said row address signals.
- 1 2. The method as recited in claim 1 wherein said reading out charge signals comprises:
2 shifting said charge signals from said set of the plurality of photo sensors,
3 respectively, to line buses in parallel;
- 1 3. The method as recited in claim 2 further comprising:
2 conditioning said charge signals to appropriate levels before being digitized in
3 parallel in a bank of analog-to-digital converters to produce pixel signals; and
4 processing said pixel signals with respect to instructions from a memory;
- 1 4. The method as recited in claim 3 wherein said processing said pixel signals is carried
2 out in a pixel processor.

1 5. The method as recited in claim 4 wherein said pixel processor and said memory are
2 monolithically integrated with said plurality of photo sensors of the CMOS image
3 sensor.

1 6. The method as recited in claim 3 wherein said conditioning said charge signals
2 comprises balancing colors in said charge signals.

1 7. The method as recited in claim 6 wherein said balancing colors comprises:
2 deriving a measurement difference of each of said charge signals with a reference;
3 and
4 adjusting said each of said charge signals with respect to said measurement
5 difference.

1 8. The method as recited in claim 2 further comprising generating an optimum exposure
2 time.

1 9. The method as recited in claim 8 wherein said generating an optimum exposure time
2 comprises:
3 deriving a measurement difference of each of said charge signals with a reference;
4 and

5 calculating said optimum exposure time from said measurement difference.

1 10. The method as recited in claim 1, wherein said set of parameters includes coordinates
2 of a region of interest and wherein said generating column signals and row signals
3 comprises:

4 identifying said set of the plurality of photo sensors corresponding to said
5 coordinates of said region of interest;

1 11. The method as recited in claim 10 wherein said processing pixel signals comprises
2 producing a larger set of digital signals by interpolating said pixel signals.

1 12. The method as recited in claim 10 wherein said processing pixel signals comprises:
2 detecting if said charge signals represent an image of a target being focused; and
3 producing a reference signal to cause said image sensor to regenerate said charge
4 signals with a new setting if said detecting indicates said target is not
5 represented well in said image.

1 16. The method as recited in claim 13 wherein said desired result is a compressed format
2 of said pixel signals and wherein said processing said pixel signals in a pixel

3 processor comprises compressing said pixel signals according to a commonly used
4 compression standard.

1 17. The method as recited in claim 16 wherein the commonly used compression standard
2 is selected from a group consisting of Graphic Interchange Format (GIF), JPEG (Joint
3 Photographic Experts Group) and MPEG (Moving Picture Experts Group) supported
4 by a World Wide Web protocol.

1 18. The method as recited in claim 13 wherein said desired result is a gray-scale intensity
2 image and wherein said processing said pixel signals in a pixel processor comprises
3 converting said pixel signals respectively to intensity data according to a predefined
4 conversion standard.

1 19. An architecture for facilitating high signal throughput of an improved CMOS image
2 sensor comprising a plurality of photo sensors configured in a two-dimensional area;
3 said architecture comprising:
4 a pair of column address and row address decoders providing address signals to
5 address each of the plurality of photo sensors;
6 a number of signal conditioning circuits, each coupled to a column data bus
7 receiving charge signals readout from said photo sensors when said photo
8 sensors are addressed by said address signals;

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9 a number of analog-to-digital converters, each respectively coupled to one of said
10 conditioning circuits and digitizing said charge signals in parallel; to produce
11 pixel signals; and
12 a pixel processor receiving said pixel signals from said analog-to-digital
13 converters, wherein said pixel signals are processed to produce a desired
14 result.

1 20. The architecture as recited in claim 19 wherein each of the signal conditioning circuits
2 comprises a correlated double sampling circuit and a programmer gain amplifier.

1 21. The architecture as recited in claim 20 wherein said correlated double sampling
2 circuit derives a measurement difference of each of said charge signals with a
3 reference.

1 22. The architecture as recited in claim 21 wherein said programmer gain amplifier
2 receives said measurement difference and adjusts said each of said charge signals with
3 respect to said measurement difference.

1 23. The architecture as recited in claim 21 wherein each of the signal conditioning circuits
2 produces a signal that indicates an optimum exposure time.

1 24. The architecture as recited in claim 23 wherein said correlated double sampling
2 circuit and said programmer gain amplifier together derives a measurement difference
3 of each of said charge signals with a reference; and calculates said optimum exposure
4 time from said measurement difference.

1 25. The architecture as recited in claim 20 further comprises a memory storing
2 instructions; said memory coupled to said pixel processor that executes said
3 instructions from said memory to achieve said desired result.

1 26. The architecture as recited in claim 25 wherein said instructions causes said pixel
2 processor to compress said pixel signals according to a commonly used compression
3 standard.

1 27. The architecture as recited in claim 26 wherein the commonly used compression
2 standard is selected from a group consisting of Graphic Interchange Format (GIF),
3 JPEG (Joint Photographic Experts Group) and MPEG (Moving Picture Experts
4 Group) supported by a World Wide Web protocol.

1 28. The architecture as recited in claim 25 wherein said instructions causes said pixel
2 processor to convert said pixel signals respectively to intensity data according to a
3 predefined conversion standard.

1 29. The architecture as recited in claim 19 wherein said pixel processor is monolithically
2 integrated with said photo sensors.

1 30. The architecture as recited in claim 20 wherein said pixel processor, said correlated
2 double sampling circuit and said programmer gain amplifier are is monolithically
3 integrated with said photo sensors.

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